Service Guide

Publication number E9340-97001
December 1999

For Safety information, Warranties, and Regulatory information,
see the pages behind the index.

Agilent Technologies LogicWave (E9340A)

The Agilent Technologies LogicWave is a 100 MHz state/250 MHz timing logic analyzer.

Features

Some of the main features of the LogicWave logic analyzer are:

- 32 data channels and 2 clock/data channels
- 128 Kbytes deep memory in timing mode, 64 Kbytes deep memory in state mode

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the E9430A.

This logic analyzer can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies sales office for more details.

The LogicWave Logic Analyzer

In This Book

This service guide for the Agilent Technologies LogicWave (E9340A) logic analyzer has the following chapters:

- Chapter 1 contains information about the logic analyzer and includes accessories, specifications and characteristics, and equipment required for servicing.
- Chapter 2 tells how to prepare the logic analyzer for use.
- Chapter 3 gives instructions on how to test the performance of the logic analyzer.
- Chapter 4 contains instructions on troubleshooting the logic analyzer.
- Chapter 5 tells how to replace logic analyzers assemblies and return them to Agilent Technologies. It also lists replaceable parts in an exploded view, and gives ordering information.

Contents

Contents

1

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

Supplied Accessories

The following accessories are supplied with the LogicWave logic analyzer.

Description	Agilent Part Number	Quantity
Probe tip assemblies	01650-61608	2
Probe cables	16550-61601	1
Grabbers (20 per pack)	5090-4356	2
Probe ground (5 per pack)	5959-9334	2

Available Accessories

The table below lists additional documentation that is available from your nearest Agilent Technologies sales office for use with your logic analyzer.

Description	Agilent Model Number
Quick Reference Card and Target Board	E9340A Option 001
Service Manual Option (this manual)	E9340A Option 0B3

Also, the LogicWave user interface software is available for download from the world-wide web at:

`http://www.agilent.com/find/LogicWave`

Specifications

Maximum state clock	100 MHz
Minimum master to master clock time*	10.0 ns
Threshold accuracy	±(100 mV + 3% of threshold setting)
Setup/hold time*	4.0/0 ns fixed

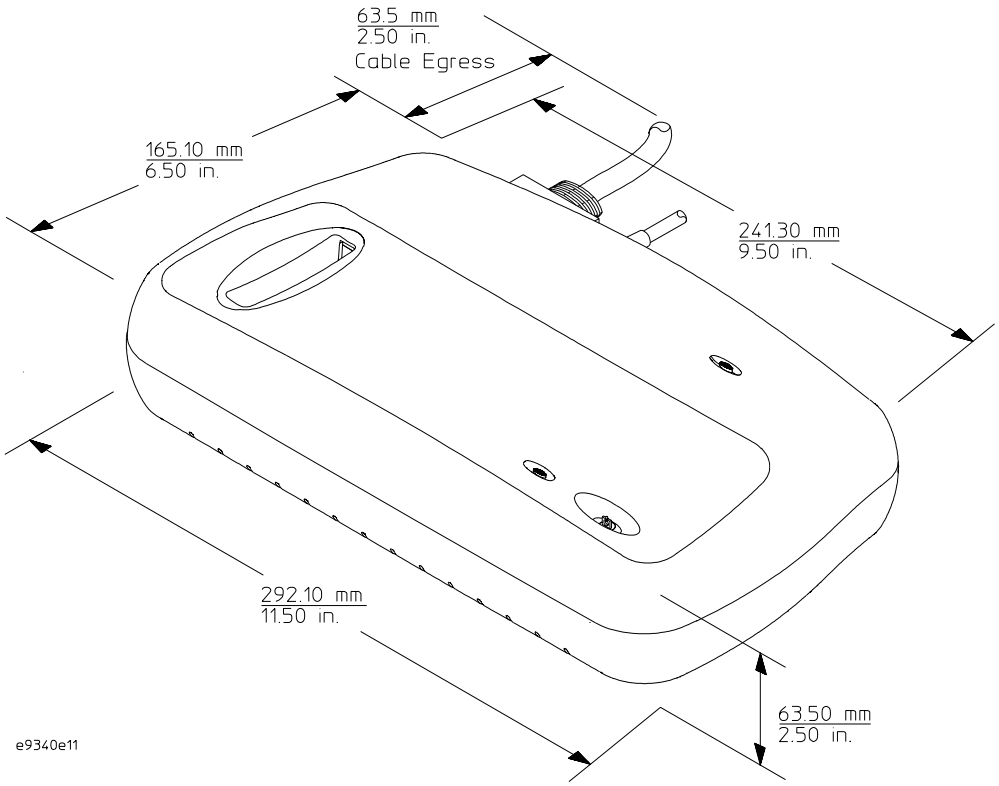
* Specified for an input signal VH = -0.9 V, VL = -1.7 V, slew rate = 1 V/ns, and threshold = -1.3 V.

Characteristics

Operating Environment

Temperature	Instrument: 0°C to 55°C (+32°F to 131°F) Disk media: 10°C to 40°C (+50°F to 104°F)
Humidity	Up to 95% relative humidity at 40°C
Altitude	4,572 m (15,000 ft)
Indoor use only	
Pollution degree 2	Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation must be expected.

Dimensions



Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/ Part Number	Use*
Pulse Generator	100 MHz, 4.0 ns pulse width, < 600 ps rise time	8133A Option 003	P, T
Digitizing Oscilloscope	6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A	P
Function Generator	Accuracy (5)(10-6) frequency, DC offset voltage ±1.5 V	3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
BNC-Banana Cable	----------	11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
Cable	BNC (m)(m) 48 inch > 2GHz bandwidth	8120-1840	P, T
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	1250-1200	P, T
Adapter	SMA(f)-BNC(m)	1250-2015	P
Coupler (Qty 4)	BNC (m)(m)	1250-0216	P, T
20:1 Probes (Qty 2)	----------	54006A	P
BNC Test Connector, 17x2 (Qty 1)**	----------	----------	P
BNC Test Connector, 6x2 (Qty 4)**	----------	----------	P, T

*A = Adjustment, P = Performance Tests, T = Troubleshooting
**Instructions for making these test connectors are in "Making the Test Connectors" on page 23

2

Preparing for Use

This chapter gives you instructions for preparing the logic analyzer for use.

Power Requirements

The logic analyzer requires a power source of either 115-230 Vac, –22% to +10%, single phase, 50-60 Hz, 100 Watts maximum power.

Operating Environment

The operating environment is listed in chapter 1. Note the noncondensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to + 75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

Accessories supplied with the logic analyzer are listed in “Supplied Accessories” on page 10.

3 Inspect the product for physical damage.

Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent

Technologies sales office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To turn on the logic analyzer

The logic analyzer user interface requires a host computer (PC) with the following characteristics (or better):

- Pentium 90 MHz
- Windows 95/98/NT
- 16MB RAM
- 10MB available space on the hard disk drive
- Available parallel port (no pass-through devices installed)
- Available LPT1 peripheral device designator

The host computer (PC) running the logic analyzer interface can be either powered on or off. The interface software is installed on the PC.

1 Connect the logic analyzer to a host computer (PC).

a Connect the small end of an HP C2946A parallel port printer cable to the PARALLEL connector on the rear panel of the logic analyzer

b Connect the large end of the printer cable to the PC's parallel port.

c Apply power to the PC if it is not turned on.

To ensure the PC's parallel port is properly configured, interrupt the PC's boot process by pressing [F2] on the keyboard. Scroll down to the parallel port configuration and observe the current parallel port data transfer mode. Ensure either Enhanced Capabilities Port (ECP), Byte, or Nibble mode is selected (Enhanced Parallel Port (EPP) mode will not work). If none of the correct transfer modes is selected, you need to change the transfer mode according to the instructions for your PC.

2 Apply power to the logic analyzer.

a Connect the power cord to the power supply input.

b Connect the power supply output cable to the power input connector on the rear panel of the logic analyzer.

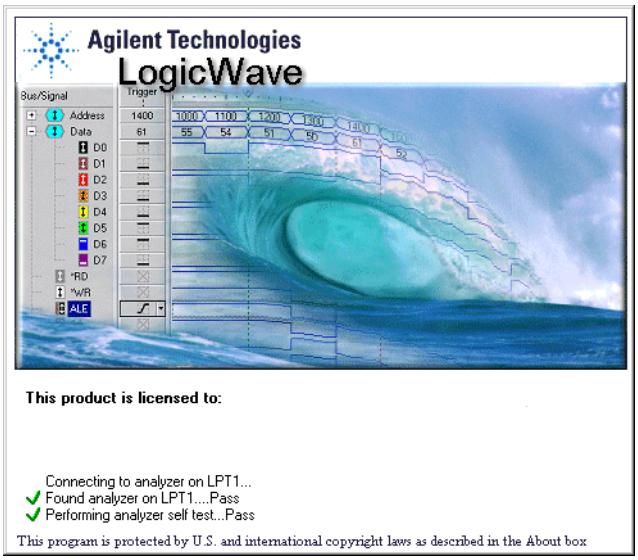
c Turn the power switch to the on ("1") position.

d Wait approximately 15 seconds for the logic analyzer to power up and settle.

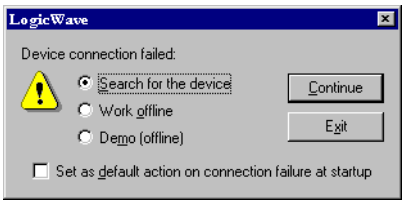
3 Start the user interface.

a Start the Agilent LogicWave application from the Start menu or using a shortcut.

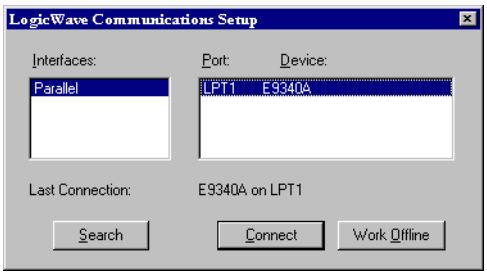
b Observe the start dialog. If the LogicWave was found, a self-test will auto-initiate and the LogicWave interface indicates “Connected”.



c If automatic connection to the logic analyzer fails, then a Device Connection Failed dialog box will appear. Select “Search for the device,” then select Continue.



d The LogicWave Communication Setup window will appear. Select the E9340A device, then select Connect.



e At the Welcome window, select Cancel.

f In the Setup Properties dialog, click OK

To clean the logic analyzer

- With the instrument turned off and unplugged, use mild soap and water to clean the cabinet of the logic analyzer.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of the "Testing Performance" chapter on page 21.
- If you require a test to initially accept the operation, see "To run the self-tests" on page 69.
- If the logic analyzer does not operate correctly, go to the the "Troubleshooting" chapter on page 65.

3

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in the “General Information” chapter on page 9.

To ensure the logic analyzer is operating as specified, you perform software tests (self-tests) and manual performance tests on the analyzer. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

Logic Analyzer User Interface

For more information on using LogicWave, refer to the online help in the user interface.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in that section.

The performance verification procedures starting with "Testing the Threshold Accuracy" on page 29 are each shown from power-up. To exactly duplicate the set-ups in the tests, save the power-up configuration to a file; then, load that configuration file at the start of each test.

If a test fails, check the test equipment set-up, check the connections, and verify adequate grounding. If a test still fails, the most probable cause of failure would be the main circuit board.

Test Interval

Test the performance of the logic analyzer against specifications at two-year intervals or if it is replaced or repaired.

Performance Test Record

Use the "Performance Test Record" on page 64 to recording the results of each test procedure and to gauge the performance of the logic analyzer over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use any equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number. Before testing the performance of the logic analyzer, warm-up the instrument and the test equipment for 30 minutes.

Making the Test Connectors

The test connectors connect the logic analyzer to the test equipment.

Materials Required

Description	Recommended Agilent Part Number	Quantity
BNC (f) Connector	1250-1032	5
100 Ω 1% resistor	0698-7212	8
Berg Strip, 17-by-2	----------	1
Berg Strip, 6-by-2	----------	4
20:1 Probe	54006A	2
Jumper wire	----------	----------

1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

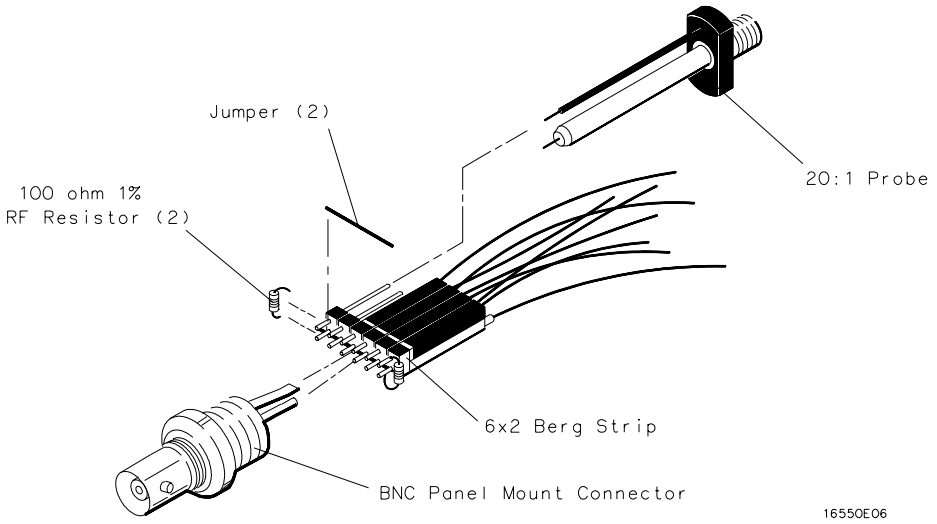
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



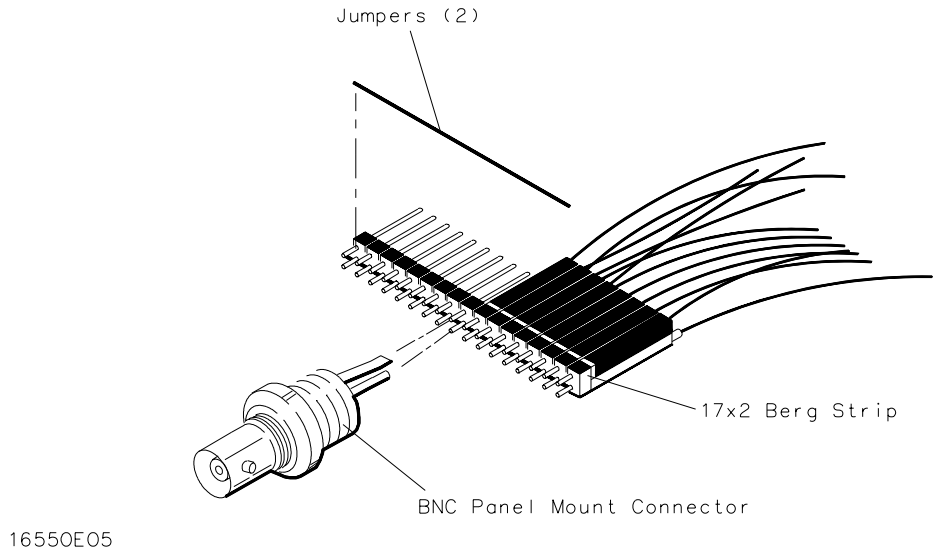
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



Setting Up the Test Equipment and the Analyzer

Before testing the specifications of the LogicWave logic analyzer, the test equipment and the logic analyzer must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analyzer. Before performing any or all of the following tests in this chapter, the steps in this section must be followed.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Number
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±1.5 V	3325B Option 002

1 Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.

2 Turn on the logic analyzer.

a Using the parallel port interface cable, connect the logic analyzer to a host computer (PC).

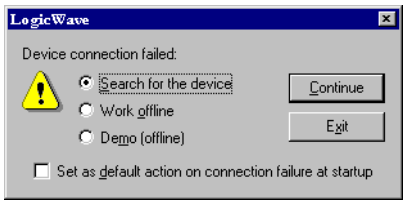
b Plug in the power cord to the power supply, and connect the power supply to the rear panel of the logic analyzer.

c Turn on the main power switch on the logic analyzer rear panel.

d Start the Agilent Logic Wave application on the host PC.

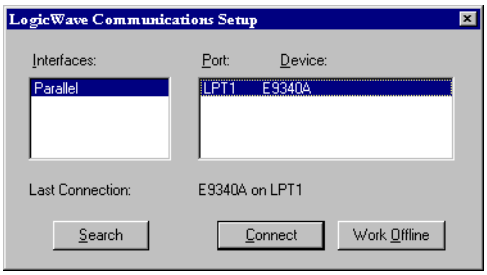
If the LogicWave was found, a self-test will auto-initiate and the LogicWave interface indicates “Connected”. If this happens, go to step 4.

e If automatic connection to the logic analyzer fails, then a Device Connection Failed dialog box will appear. Select “Search for the device,” then select Continue.



f The LogicWave Communication Setup window will appear. Select the

E9340A device, then select Connect.



g At the Welcome window, select Cancel.

3 If the self-tests are not run when starting the user interface, choose the Tools->Self Test... command.

If the self-tests pass, a confirmation dialog appears.

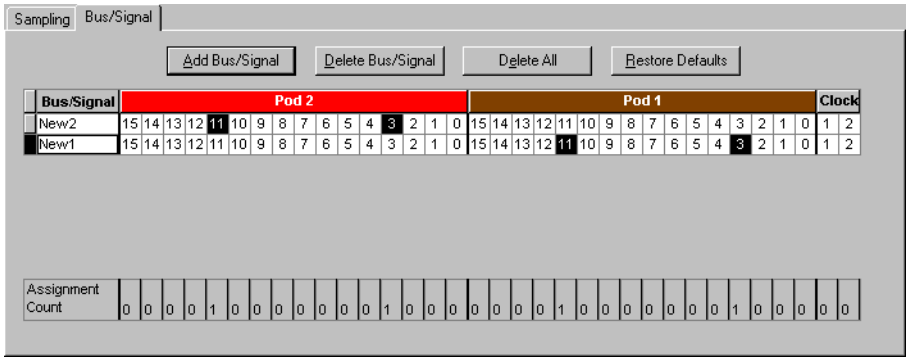
If the self-tests fail, the logic analyzer assembly requires replacement.

4 Configure the Setup Properties (do this step before the state acquisition mode tests).

a Select Bus/Signal, then select Setup.

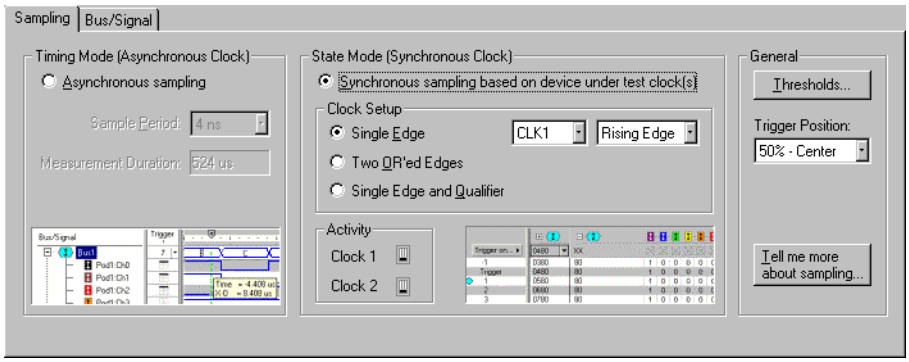
b Select the Delete All button. Then click the Add Bus/Signal button two times.

c Assign channel 3 and channel 11 from Pod 1 to the New1 label. Assign channel 3 and channel 11 from Pod 2 to the New2 label.

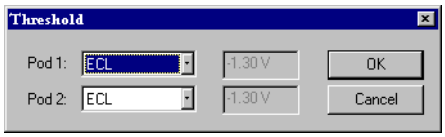


d Select the Sampling tab.

e Under the Sampling tab, select State Mode - Synchronous sampling.

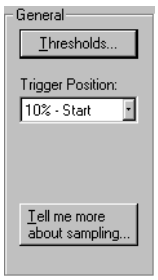


f Select the Thresholds button. In the Threshold window, select the threshold field for Pod 1, then select ECL. Repeat for Pod 2.



Select the OK button to close the Threshold window.

g Select the Trigger Position field, then select 10% - Start.



h Select OK to close the Setup Properties window.

5 Set up the pulse generator according to the following table.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 10.000 ns	Mode: Pulse Divide: Pulse ÷ 2 Width: 4.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)

6 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	Display	Timebase	Trigger	[Shift] Δ Time
Averaging: On # of averages: 16	Graticule graphs: 2	Scale: 2.0 ns/div	Level: 0.0 mV	Stop src: channel 2 [Enter]

Channel 1	Channel 2	Define meas
External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	Thresholds: user-defined Units: Volts Upper: - 980 mV Middle: -1.30 V Lower: -1.62 V

Allow the logic analyzer to warm up for 30 minutes before beginning any of the following tests.

Testing the Threshold Accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test pod 2. To test pod 2, follow the detailed steps for pod 1, substituting the pod 2 for pod 1 in the instructions.

Each threshold test tells you to record a PASS/FAIL in the "Performance Test Record" on page 64.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Numbers
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±1.5 V	3325B Option 002
BNC-Banana Cable	----------	11001-60001
BNC Tee	----------	1250-0781
BNC Cable	----------	8120-1840
BNC Test Connector, 17x2	----------	----------

Set up the equipment

1 Set up the function generator.

a Set up the function generator to provide a DC offset voltage at the Main Signal output.

b Disable any AC voltage to the function generator output, and enable the high voltage output.

c Monitor the function generator DC output voltage with the multimeter.

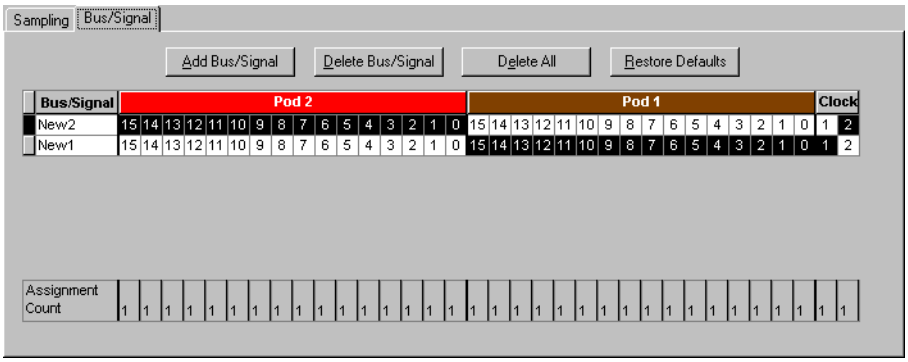
Set up the logic analyzer

1 1 Configure the Setup Properties.

a Select Bus/Signal, then select Setup.

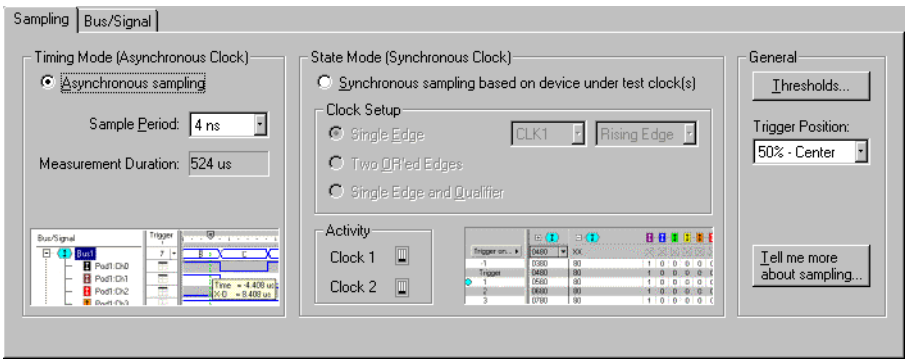
b Select the Delete All button. Then click the Add Bus/Signal button two times.

c Assign all Pod 1 channels and Clock 1 to the New1 label. Assign all Pod 2 channels and Clock 2 to the New2 label.



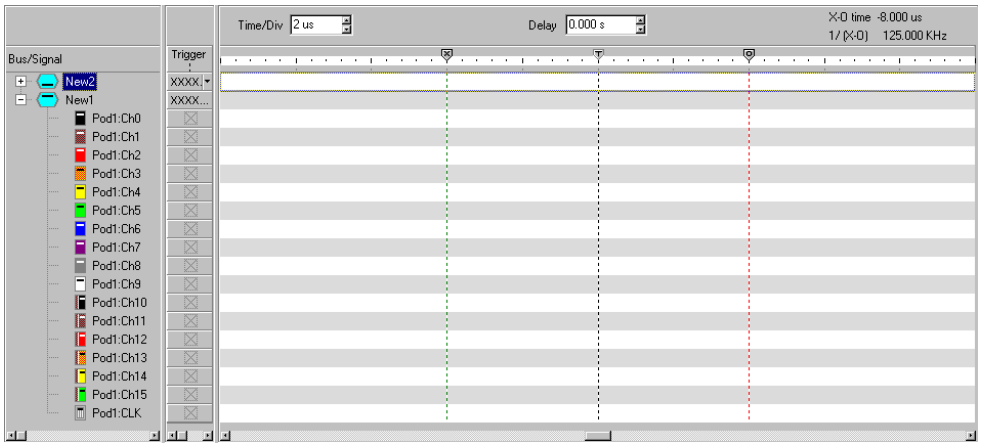
d Select the Sampling tab.

e Under the Sampling tab, select Timing Mode - Asynchronous sampling.



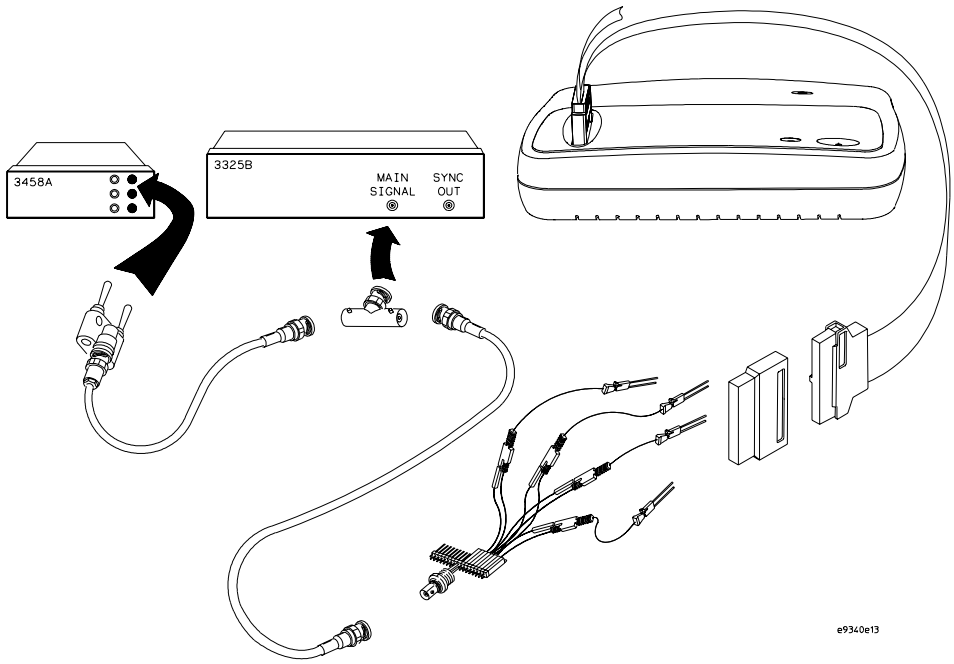
f Select OK to close the Setup Properties window.

g In the main Waveform View window, click the [-] next to the New2 label to collapse the individual New2 channels.



Connect the logic analyzer

1. Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of pod 1 to one side of the BNC Tee.
2. Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.
3. Connect the BNC Tee to the Main Signal output of the function generator.



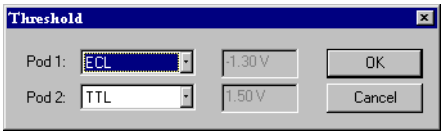
Test the ECL threshold

1 Set the logic analyzer Pod 1 threshold to ECL.

a Select Data; then, select Sampling Setup.

b Under the Sampling tab, select the Thresholds button.

c At the pop-up menu, select the Pod 1 threshold field, then select ECL.



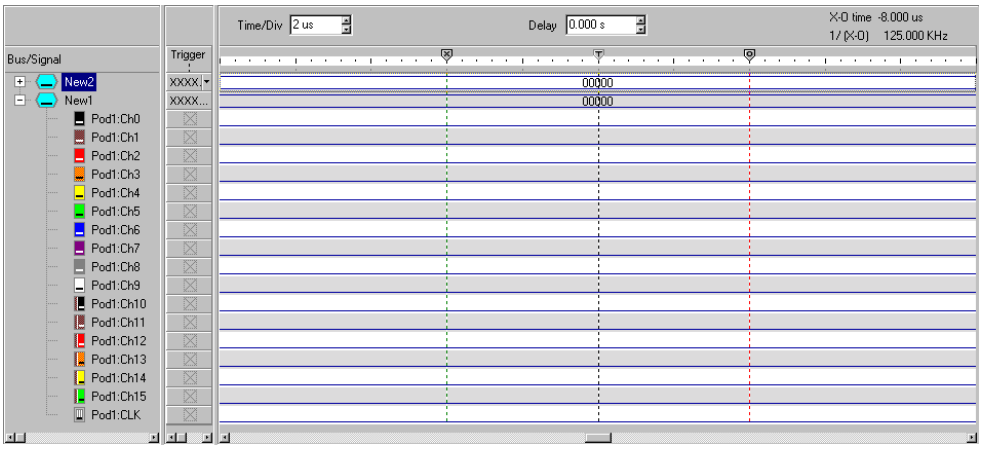
d Select OK to close the threshold window.

e Select OK to close the Setup Properties window.

2 Test the high-to-low transition.

a On the DC power source, enter -1.438 V.

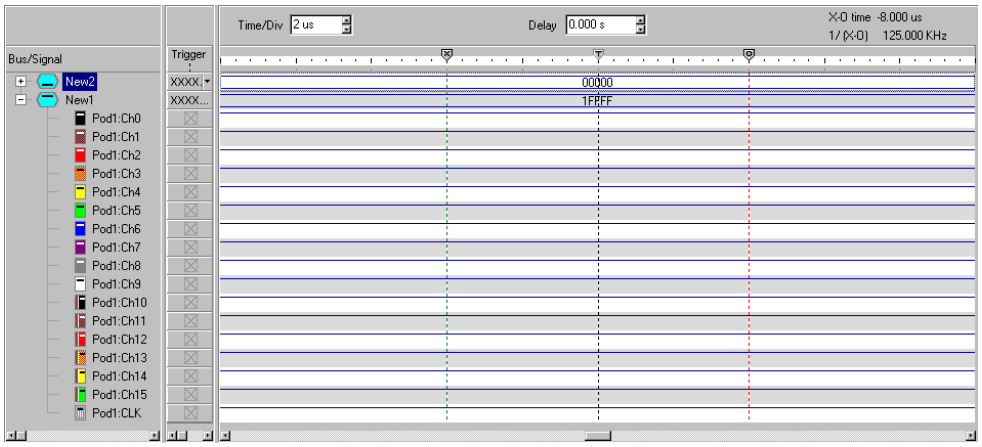
b On the PC, push the F5 key to Run. The display should show all Pod 1 channels (label New1) at a logic “0”.



3 Test the low-to-high transition.

a On the DC power source, enter -1.162 V.

b On the PC, push the F5 key to Run. The display should show all Pod 1 channels (label New1) at a logic “1”.



Test the 0 V User threshold

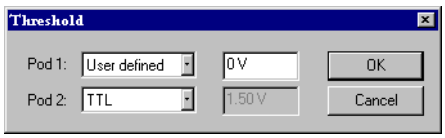
1 Set the logic analyzer Pod 1 threshold to 0 V.

a Select Data; then, select Sampling Setup.

b Under the Sampling tab, select the Thresholds button.

c At the pop-up menu, select the Pod 1 threshold field, then select User defined.

d In the threshold voltage field, enter 0 V.



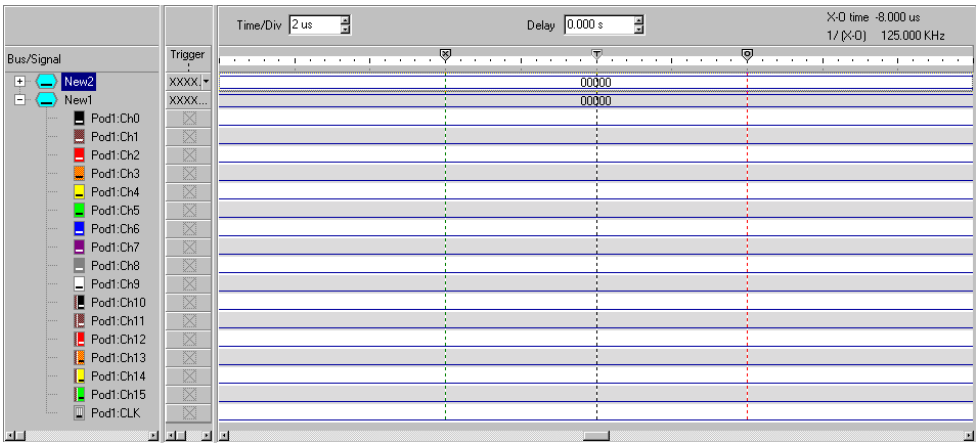
e Select OK to close the threshold window.

f Select OK to close the Setup Properties window.

2 Test the high-to-low transition.

a On the DC power source, enter -0.099 V.

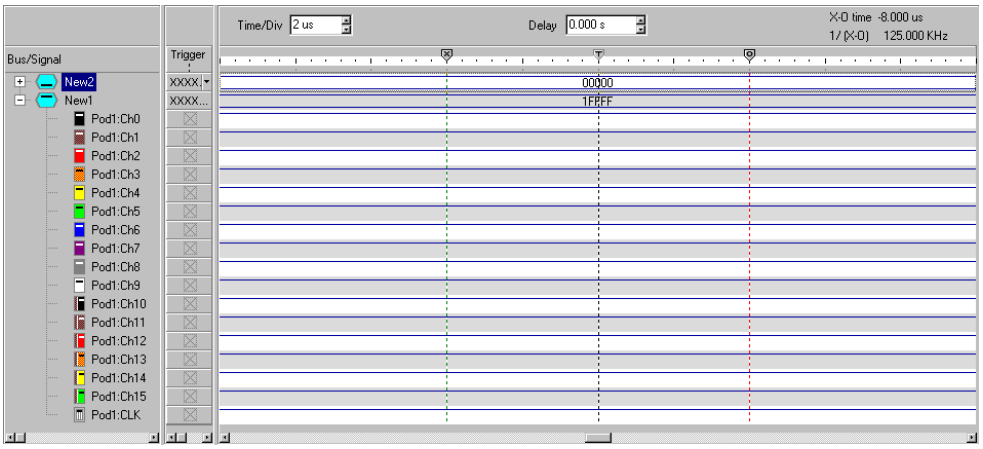
b On the PC, push the F5 key to Run. The display should show all Pod 1 channels (label New1) at a logic “0”.



3 Test the low-to-high transition.

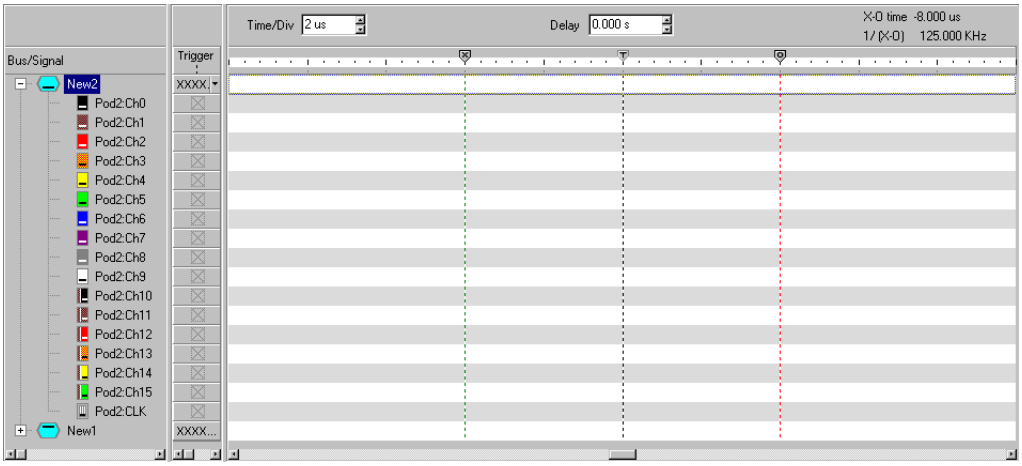
a On the DC power source, enter 0.099 V.

b On the PC, push the F5 key to Run. The display should show all Pod 1 channels (label New1) at a logic “1”.



Test Pod 2 thresholds

1 In the main Waveform View window, click the [+] next to the New2 label to expand the individual channels. Click the [-] next to the New1 label to collapse the individual channels.



2 Repeat both Test the ECL threshold and Test the 0 V User threshold substituting Pod 2 for Pod 1 and label New2 for New1

Testing Single-Clock, Single-Edge, State Acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for single-clock, single-edge, state acquisition.

This test checks the data channels using a single-edge clock.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Numbers
Pulse Generator	100 MHz 4.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	6 GHz bandwidth, < 58 ps rise time	54750A with 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
BNC Cable	BNC(m)(m) 48 in. >2 GHz bandwidth	8120-1840
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)	----------	----------

Set up the equipment

- If you have not already done so, do the procedure “Setting Up the Test Equipment and the Analyzer” on page 25. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

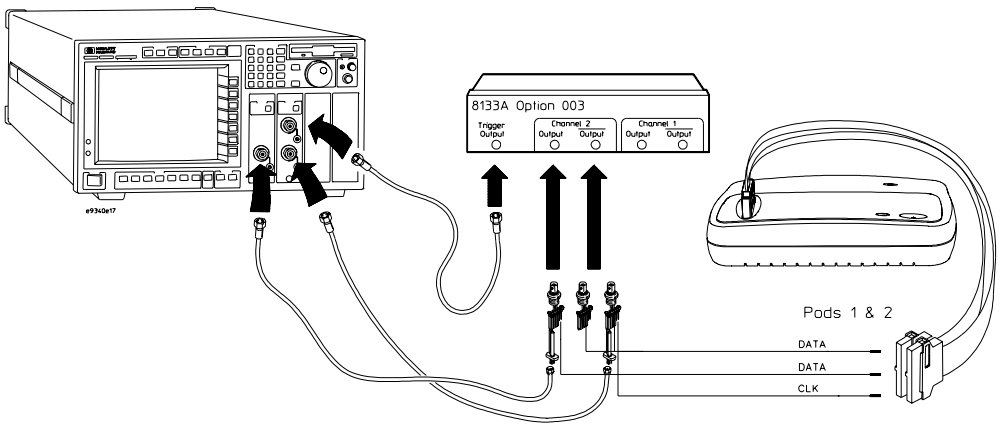
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following table to the pulse generator. Install a BNC cable between the pulse generator channel 2 output and the 6x2 test connector with the logic analyzer clock leads.

2 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trig Output.

Connect the Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3	Pod 1, channel 11 Pod 2, channel 11	CLK1 (Pod 1 clock)



Verify the test signal

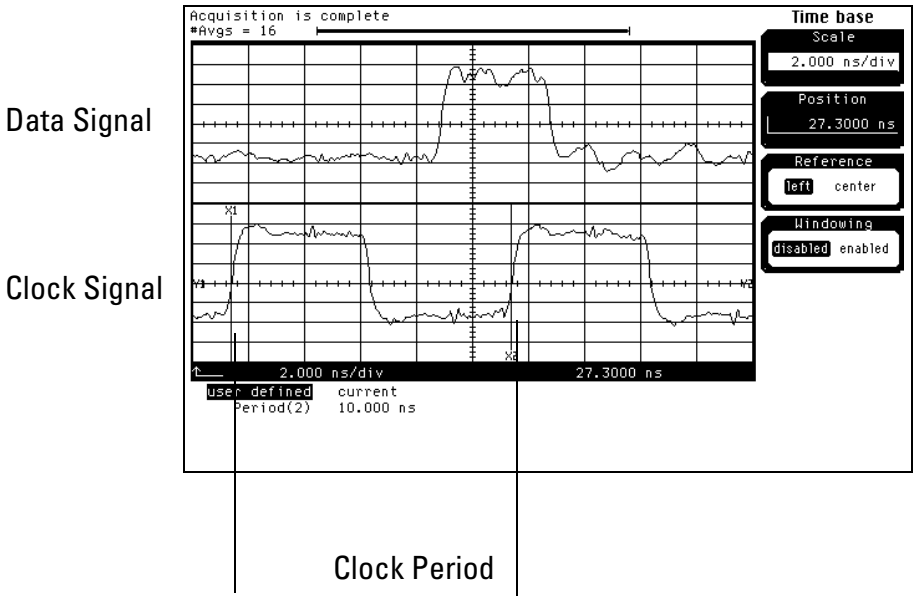
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 10.000 ns but greater than 9.750 ns.

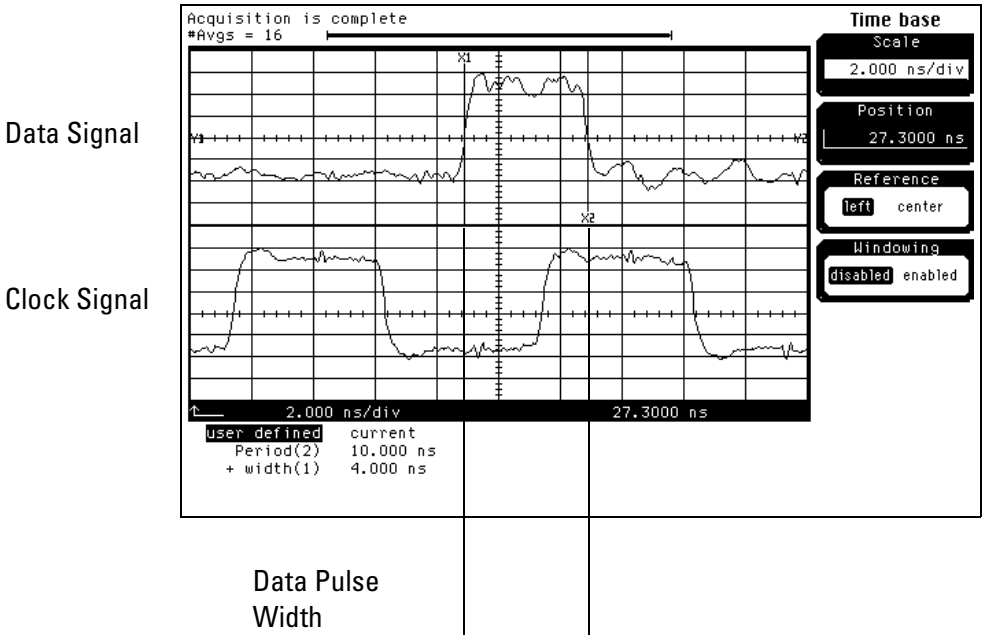


2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or -50 ps.

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



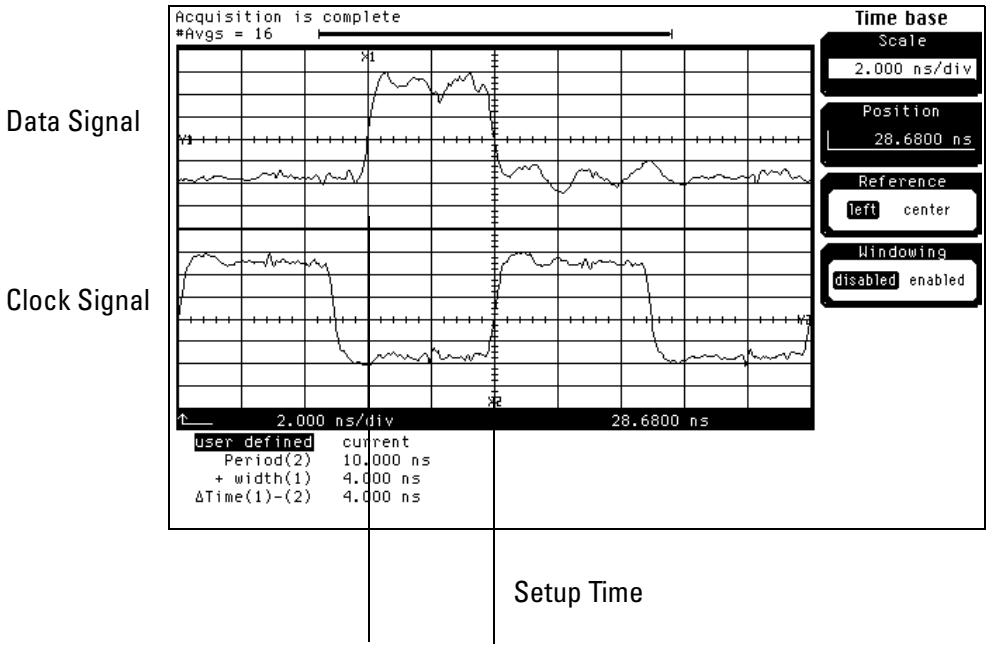
3 Using the Delay mode of the pulse generator channel 1, position the pulses for 4.0/0.0 ns setup/hold combination, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to a setup time of 4.000 ns, +0.0 ps or -100 ps



Verify the test data

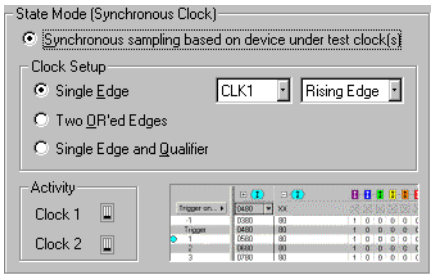
1 Assign the state clock to CLK1 Rising.

a Select Data. At the pop-up menu, select Sampling Setup.

b Under the State Mode section of the window, select Clock Setup - Single Edge.

c Select the clock assignment field, then select CLK1.

d Select the edge field, then select Rising Edge.



e Select the OK button to close the window.

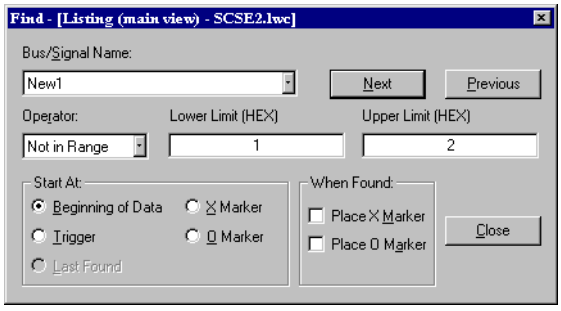
2 Acquire and analyze the data.

a On the PC, push the F5 key to Run.

b On the PC, select Data, then select Find Data Value.

c In the Find Data Value window, select the Operator field, then select Not In Range. In the Lower Limit field, enter “1”. In the Upper Limit field, enter “2”.

d In the Start At: field, select Beginning of Data.



e Select the Next button. If the “Not Found” message appears, select OK to close the “Not Found” message box.

f Select the Bus/Signal Name field, then select New2. Select the Next button. If the "Not Found" message appears, select OK to close the "Not Found" message box.

If the "Not Found" message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK1 Rising PASS/FAIL in the "Performance Test Record" on page 64.

g Select Close to close the Find Data Value window.

3 Assign the state clock to CLK2 Rising

a Select Data. At the pop-up menu, select Sampling Setup.

b Select the clock assignment field, then select CLK2.

c Disconnect the pod 1 clock channel (CLK1) from the pulse generator channel 1 output and connect the Pod 2 clock channel (CLK2).

d Select the OK button to close the window.

e Repeat step 2 above to verify the data.

If the "Not Found" message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK2 Rising PASS/FAIL in the "Performance Test Record" on page 64.

4 Set up the pulse generator to test falling clock edges.

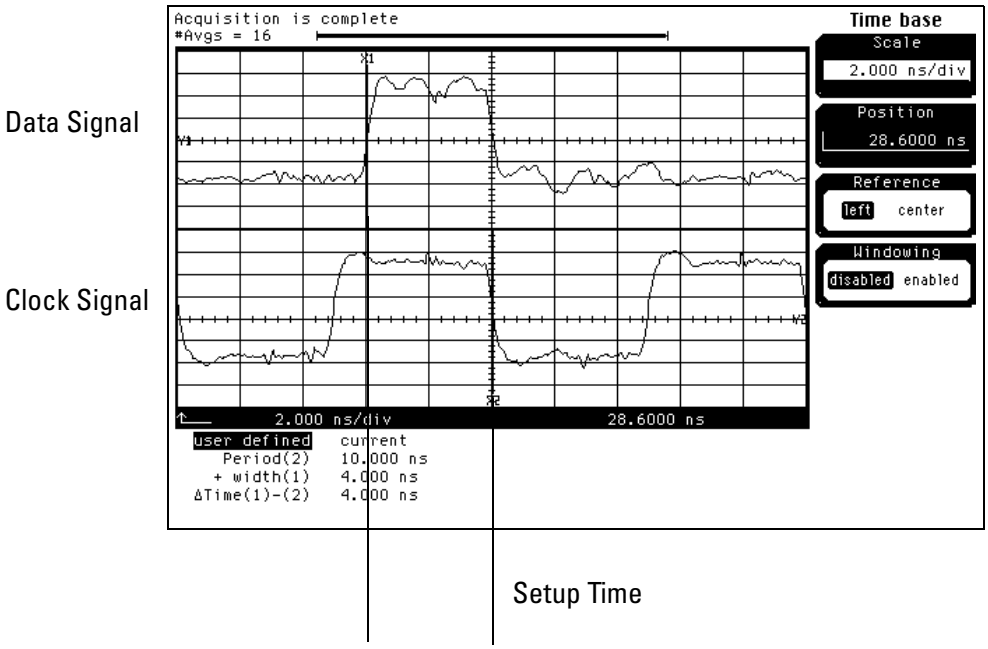
a Enable the pulse generator channel 1 COMP (LED on)

b Check the data pulse width. On the oscilloscope, select [Shift] - width: channel 1, then select [Enter] to display the data signal pulse width (-width(1).

c If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the measured pulse width is 4.000 ns +0 ps or -100 ps.

d On the oscilloscope, select [Define Meas] Define ΔTime - Stop Edge: falling.

e On the oscilloscope, select [Shift] ΔTime, then select [Enter] to display the setup time (ΔTime(1)-(2)). Adjust the pulse generator channel 2 Delay for a setup time of 4.000 ns +0 ps or -100 ps.

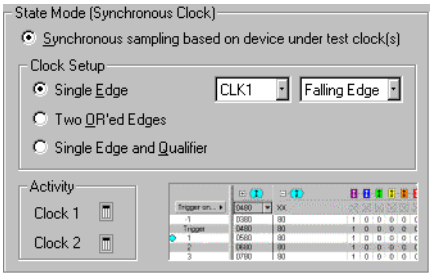


5 Assign the state clock to CLK1 Falling.

a Select Data. At the pop-up menu, select Sampling Setup.

b Select the clock assignment field, then select CLK1.

c Select the edge field, then select Falling Edge.



d Select the OK button to close the window.

e Disconnect the Pod 2 clock channel (CLK2) from the pulse generator channel 1 output and connect the pod 1 clock channel (CLK1).

f Repeat step 2 above to verify the data.

If the “Not Found” message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK1 Falling PASS/FAIL in the “Performance Test Record” on page 64.

6 Assign the state clock to CLK2 Falling.

a Select Data. At the pop-up menu, select Sampling Setup.

b Select the clock assignment field, then select CLK2.

c Disconnect the pod 1 clock channel (CLK1) from the pulse generator channel 1 output and connect the Pod 2 clock channel (CLK2).

d Select the OK button to close the window.

e Repeat step 2 above to verify the data.

If the “Not Found” message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK2 Falling PASS/FAIL in the “Performance Test Record” on page 64.

7 Disable the pulse generator channel 1 COMP (LED off).

Testing Multiple-Clock, Multiple-Edge, State Acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for multiple-clock, multiple-edge, state acquisition.

This test checks data using multiple clocks.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Number
Pulse Generator	100 MHz 4.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
BNC Cable	BNC(m)(m) 48 in. > 2 GHz bandwidth	8120-1840
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)	----------	----------

Set up the equipment

- If you have not already done so, do the procedure "Setting Up the Test Equipment and the Analyzer" on page 25. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

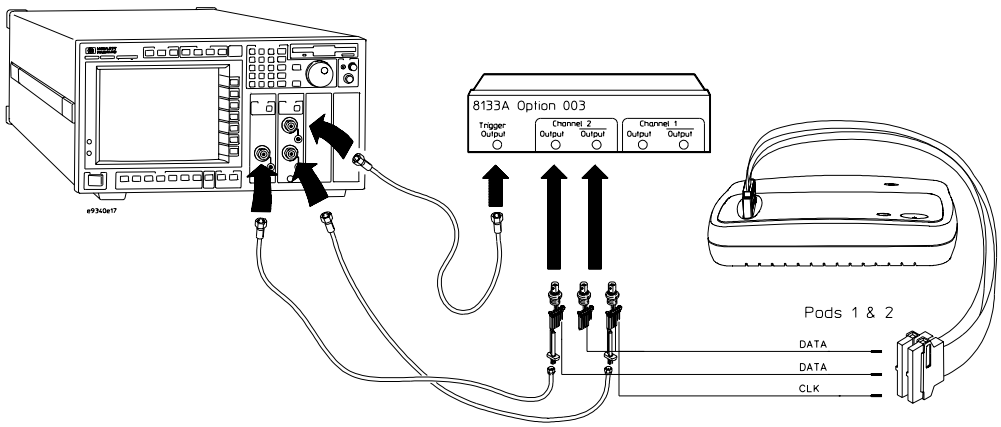
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following table to the pulse generator. Install a BNC cable between the pulse generator channel 2 output and the 6x2 test connector with the logic analyzer clock leads.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3	Pod 1, channel 11 Pod 2, channel 11	CLK1 (Pod 1 clock) CLK2 (Pod 2 clock)



Verify the test signal

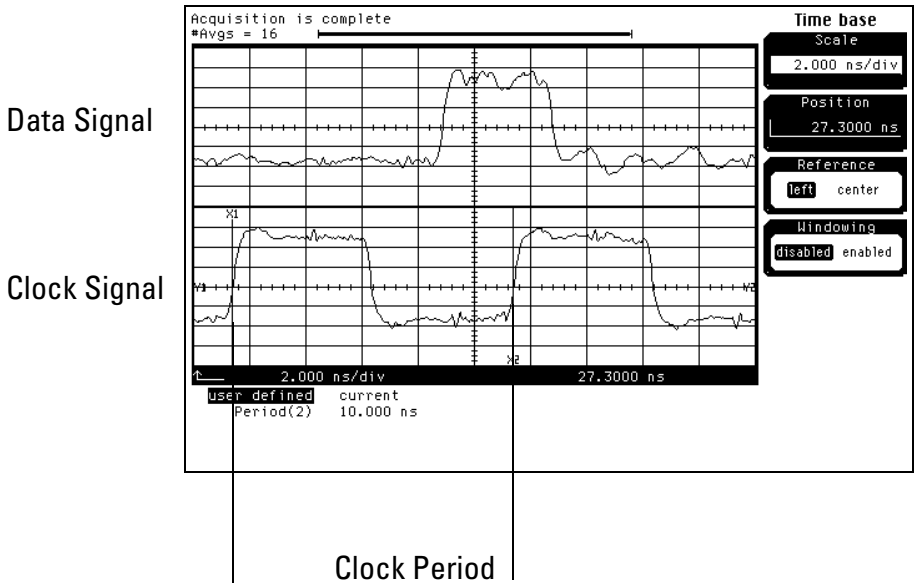
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.

d In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 10.000 ns but greater than 9.750 ns.

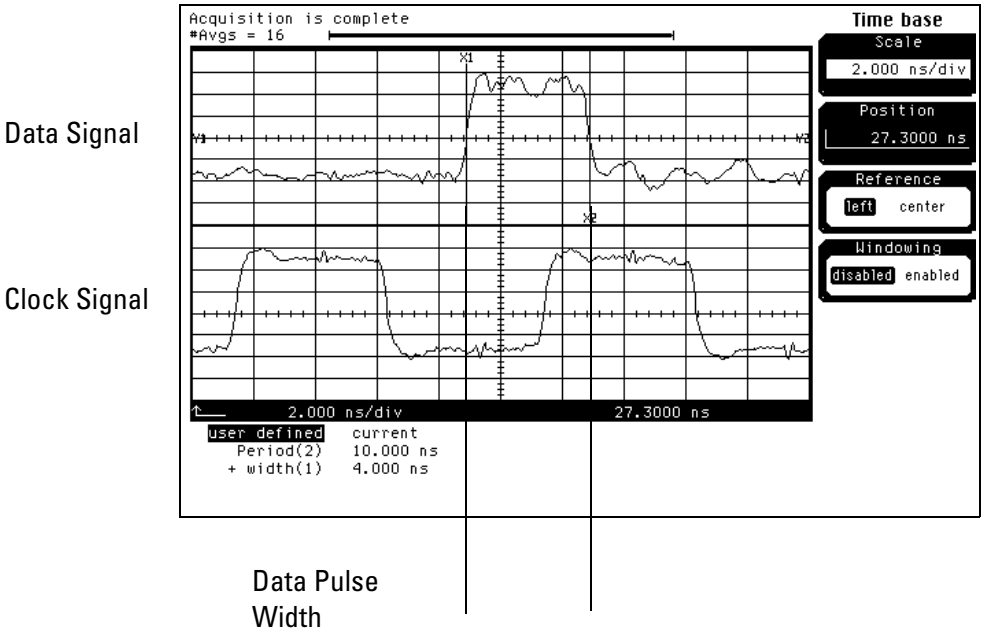


2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or -50 ps.

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



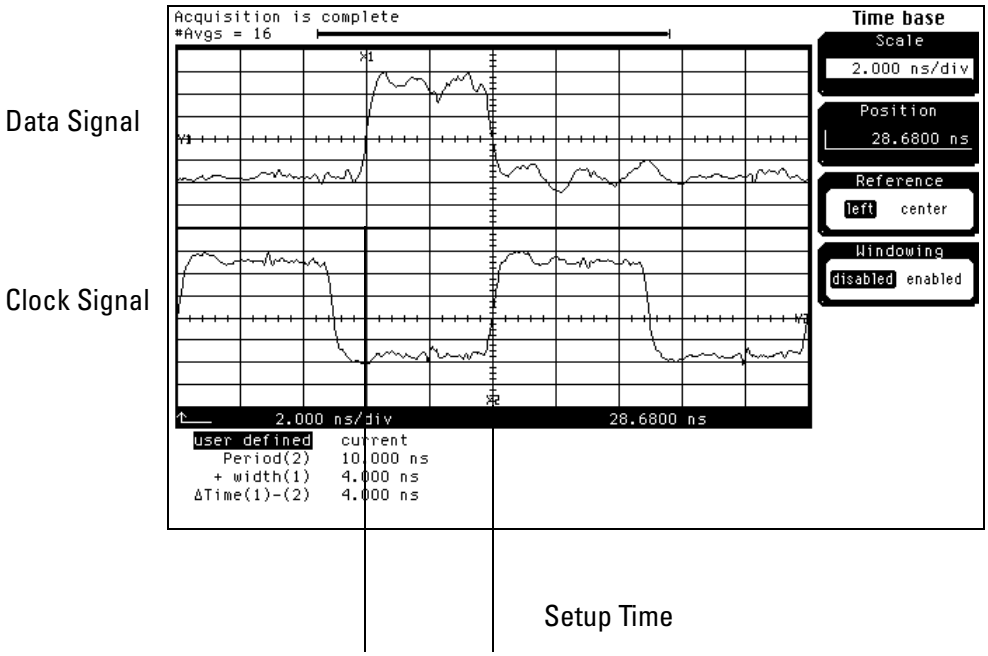
3 Using the Delay mode of the pulse generator channel 1, position the pulses for 4.0/0.0 ns setup/hold combination, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to a setup time of 4.000 ns, +0.0 ps or -100 ps



Verify the test data

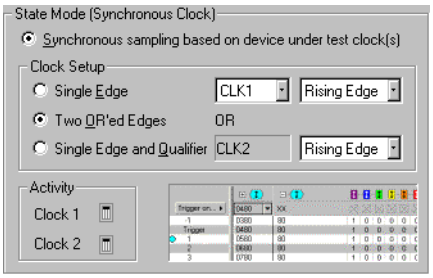
1 Assign the state clock to CLK1 or CLK2 Rising.

a Select Data. At the pop-up menu, select Sampling Setup.

b Under the State Mode section of the window, select Clock Setup - Two OR'ed Edges.

c Select the clock assignment field, then select CLK1.

d Select the CLK1 edge field, then select Rising Edge. Select the CLK2 edge field, then select Rising Edge.



e Select the OK button to close the window.

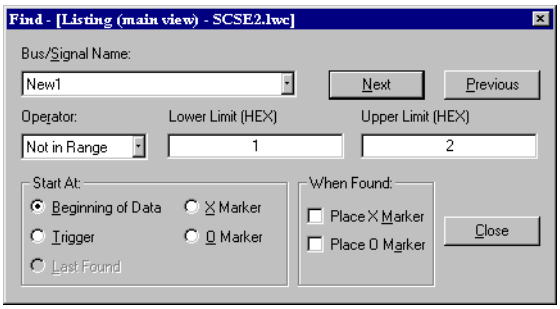
2 Acquire and analyze the data.

a On the PC, push the F5 key to Run.

b On the PC, select Data, then select Find Data Value.

c In the Find Data Value window, select the Operator field, then select Not In Range. In the Lower Limit field, enter "1". In the Upper Limit field, enter "2".

d In the Start At: field, select Beginning of Data.



e Select the Next button. If the "Not Found" message appears, select OK to close the "Not Found" message box.

f Select the Bus/Signal Name field, then select New2. Select the Next button. If the "Not Found" message appears, select OK to close the "Not Found" message box.

If the "Not Found" message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK1 OR CLK2 Rising PASS/FAIL in the "Performance Test Record" on page 64.

3 Set up the pulse generator to test falling clock edges.

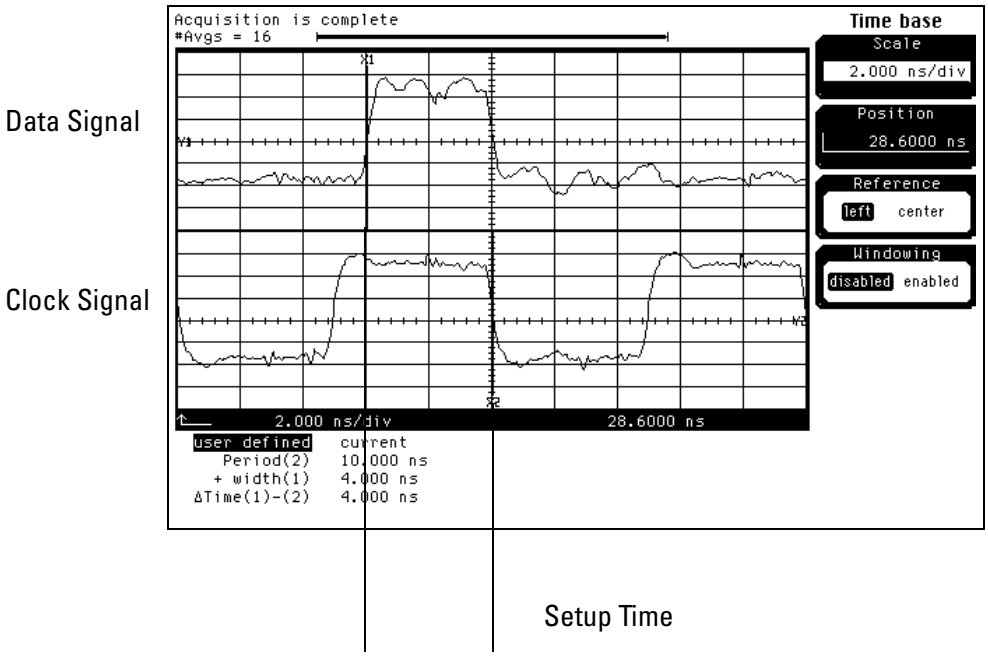
a Enable the pulse generator channel 1 COMP (LED on)

b Check the data pulse width. On the oscilloscope, select [Shift] - width: channel 1, then select [Enter] to display the data signal pulse width (-width(1).

c If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the measured pulse width is 4.000 ns +0 ps or -100 ps.

d On the oscilloscope, select [Define Meas] Define ΔTime - Stop Edge: rising.

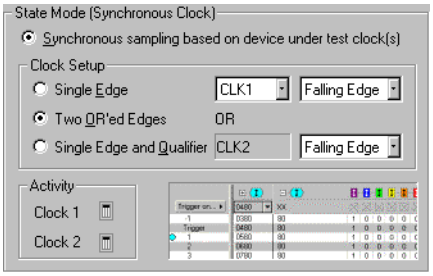
e On the oscilloscope, select [Shift] ΔTime, then select [Enter] to display the setup time (ΔTime(1)-(2)). Adjust the pulse generator channel 2 Delay for a setup time of 4.000 ns +0 ps or -100 ps.



4 Assign the state clock to CLK1 OR CLK2 Falling.

a Select Data. At the pop-up menu, select Sampling Setup.

b Select the CLK1 edge field, then select Falling Edge. Select the CLK2 edge field, then select Falling Edge.



c Select the OK button to close the window.

d Repeat step 2 above to verify the data.

If the “Not Found” message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK1 OR CLK2 Falling PASS/FAIL in the “Performance Test Record” on page 64.

Testing Single-Clock, Multiple-Edge, State Acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for single-clock, multiple-edge, state acquisition.

This test checks data channels using a multiple-edge single clock.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Number
Pulse Generator	100 MHz 4.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
BNC Cable	BNC(m)(m) 48 in. >2 GHz bandwidth	8120-1840
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)	----------	----------

Set up the equipment

1 If you have not already done so, do the procedure "Setting Up the Test Equipment and the Analyzer" on page 25. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

2 Make the following changes to the pulse generator configuration.

Timebase	Channel 2
Period: 20.000 ns	Divide: PULSE ÷ 1

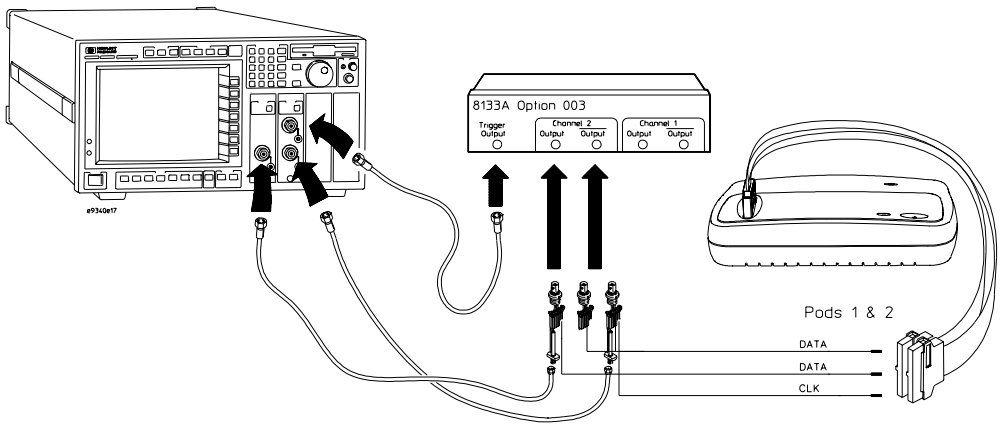
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following table to the pulse generator. Install a BNC cable between the pulse generator channel 2 output and the 6x2 test connector with the logic analyzer clock leads.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3	Pod 1, channel 11 Pod 2, channel 11	CLK1 (Pod 1 clock)



Verify the test signal

1 Check the clock interval. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

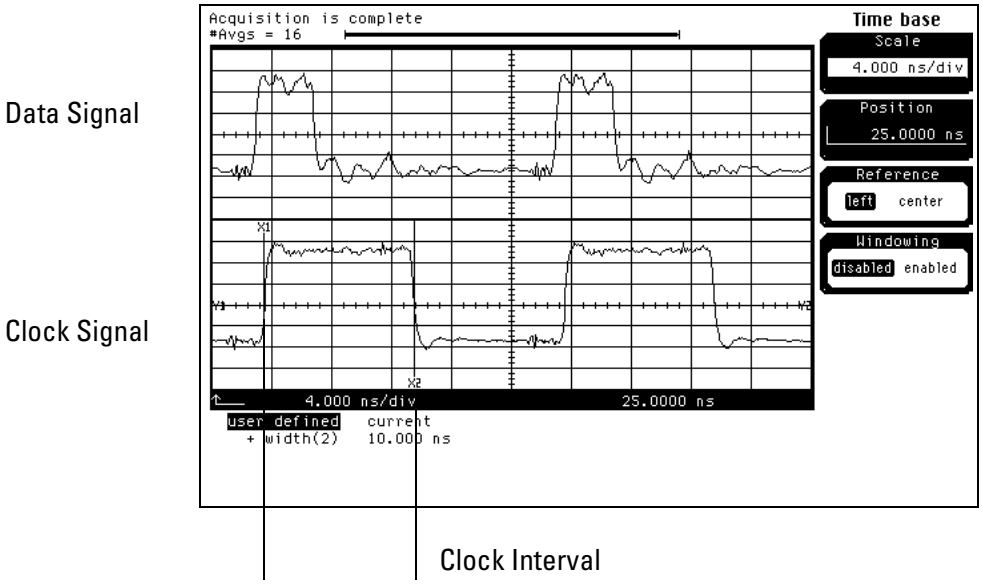
b In the oscilloscope Timebase menu, select Scale: 4.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 10.000 ns, go to step e. If the positive-going pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.

e On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.

f Decrease the pulse generator Period in 10-ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 10.000 ns, but greater than 9.750 ns.



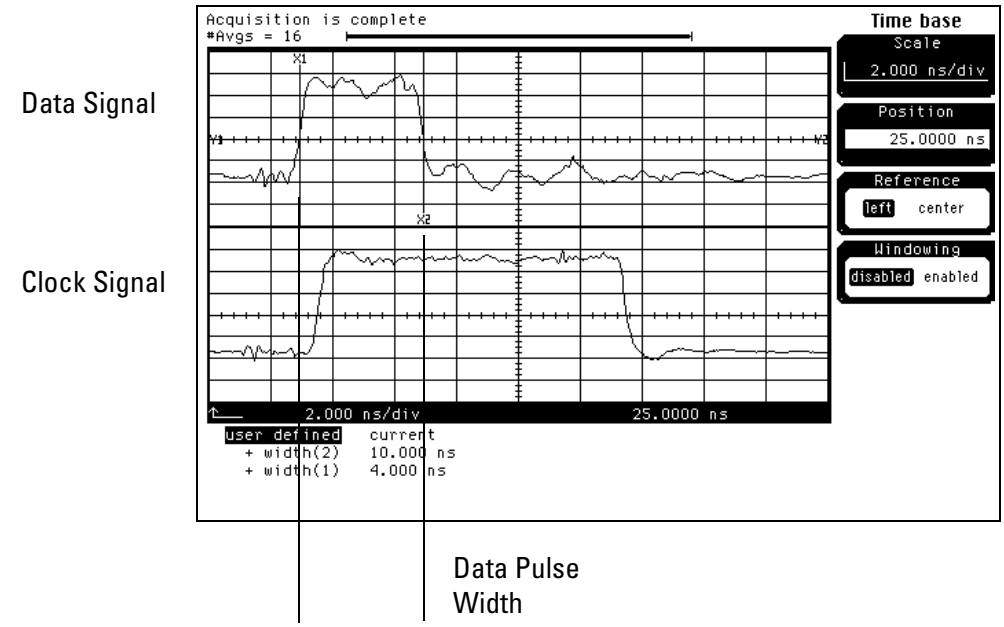
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



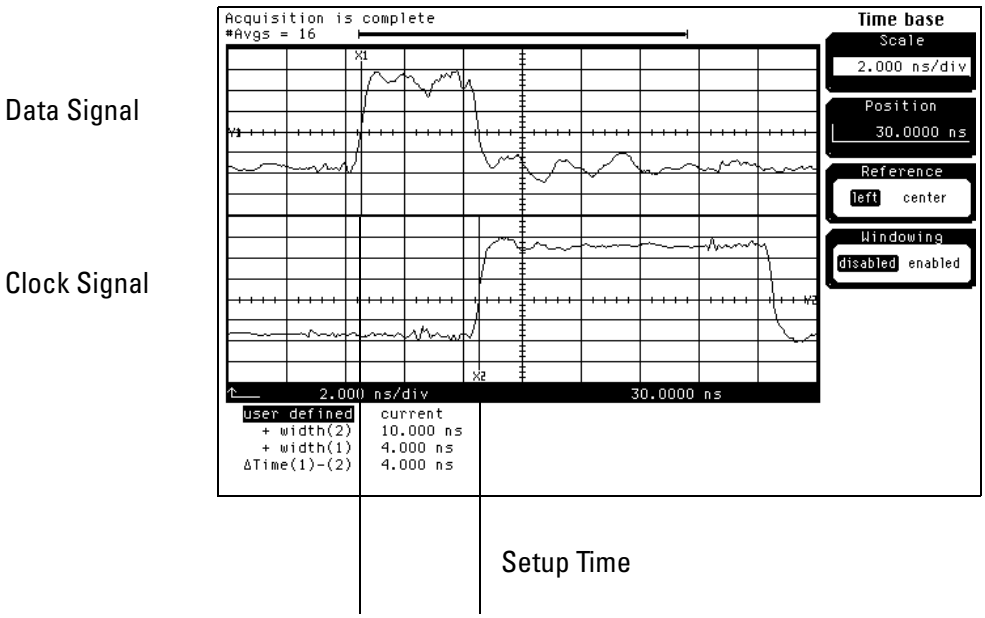
3 Using the Delay mode of the pulse generator channel 1, position the pulses for 4.0/0.0 ns setup/hold combination, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 2 Delay until the pulses are aligned according a setup time of 4.000 ns, +0.0 ps or -100 ps.



Verify the test data

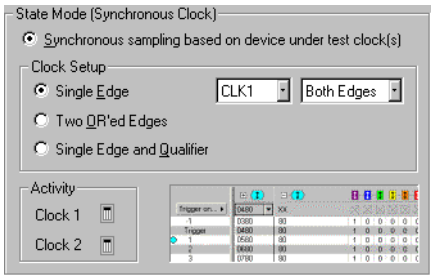
1 Assign the state clock to CLK1 Both Edges.

a Select Data. At the pop-up menu, select Sampling Setup.

b Under the State Mode section of the window, select Clock Setup - Single Edge.

c Select the clock assignment field, then select CLK1.

d Select the edge field, then select Both Edges.



e Select the OK button to close the window.

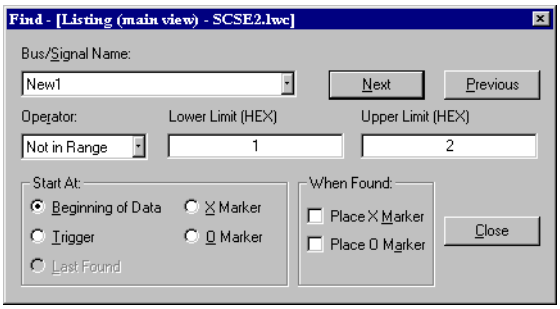
2 Acquire and analyze the data.

a On the PC, push the F5 key to Run.

b On the PC, select Data, then select Find Data Value.

c In the Find Data Value window, select the Operator field, then select Not In Range. In the Lower Limit field, enter “1”. In the Upper Limit field, enter “2”.

d In the Start At: field, select Beginning of Data.



e Select the Next button. If the “Not Found” message appears, select OK to close the “Not Found” message box.

f Select the Bus/Signal Name field, then select New2. Select the Next button. If the “Not Found” message appears, select OK to close the “Not Found” message box.

If the “Not Found” message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK1 Both Edges PASS/FAIL in the “Performance Test Record” on page 64.

3 Assign the state clock to CLK2 Both Edges

a Select Data. At the pop-up menu, select Sampling Setup.

b Select the clock assignment field, then select CLK2.

c Disconnect the Pod 1 clock channel (CLK1) from the pulse generator channel 1 output and connect the Pod 2 clock channel (CLK2).

d Repeat step 2 above to verify the data.

If the “Not Found” message appears for both step 2-e and step 2-f above, the test passes. Record a Single Clock-Single Edge CLK2 Both Edges PASS/FAIL in the “Performance Test Record” on page 64.

Testing the Time Interval Accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125 MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Number
Pulse Generator	100 Mhz, 4.0 ns pulse width, < 600 ps rise time	8133A Option 003
Function Generator	Accuracy ≤ (5)(10^{-6}) x frequency	8656B Option 002
SMA Coax Cable	18 GHz Bandwidth	8120-4948
BNC Cable	----------	8120-1840
Adapter	SMA(m)-BNC(f)	1250-1200
Adapter	BNC(m)-SMA(f)	1250-2015
Coupler	BNC(m-m)	1250-0216
BNC Test Connector, 6x2	----------	----------

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2. Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

3 Set up the function generator according to the following table.

Function Generator Setup

Freq: 40.000 00 MHz	Amptd: 1.00 V	Modulation: Off

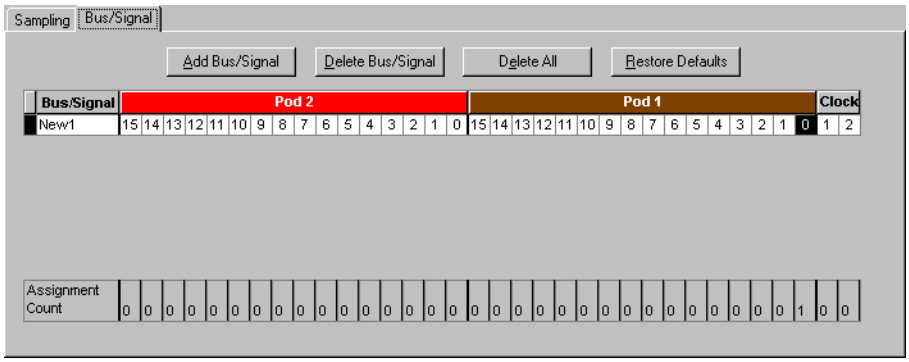
Set up the logic analyzer

1 Configure the Setup Properties.

a Select Bus/Signal, then select Setup.

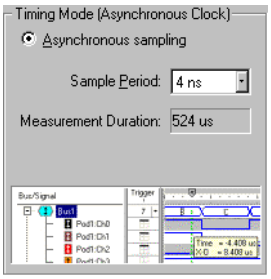
b Select the Delete All button. Then click the Add Bus/Signal button one time.

c Assign channel 0 from Pod 1 to the New1 label.

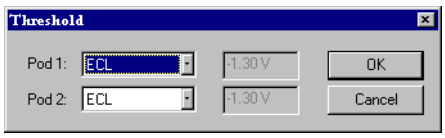


d Select the Sampling tab.

e Under the Sampling tab, select Timing Mode - Asynchronous sampling.

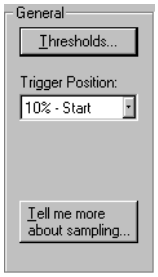


f Select the Thresholds button. In the Threshold window, select the threshold field for Pod 1, then select ECL.



Select the OK button to close the Threshold window.

g Select the Trigger Position field, then select 10% - Start.

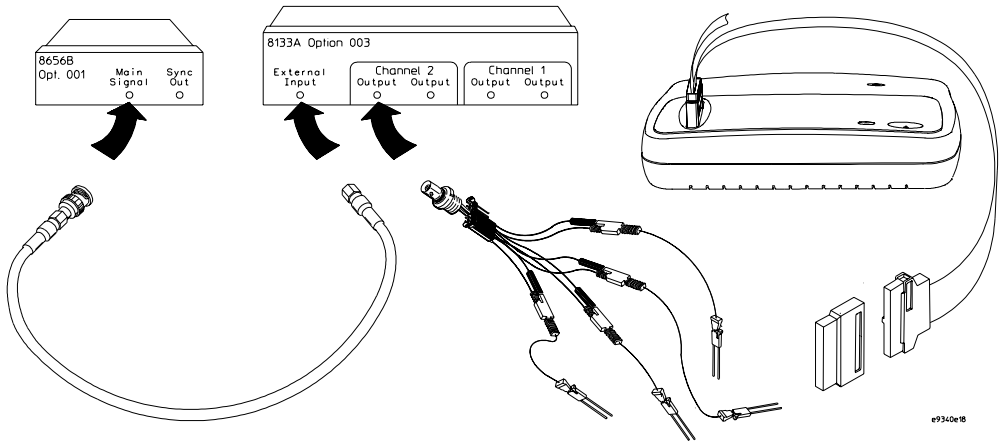


h Select OK to close the Setup Properties window.

Connect the logic analyzer

1 Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 1 output.

2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



Verify the test data

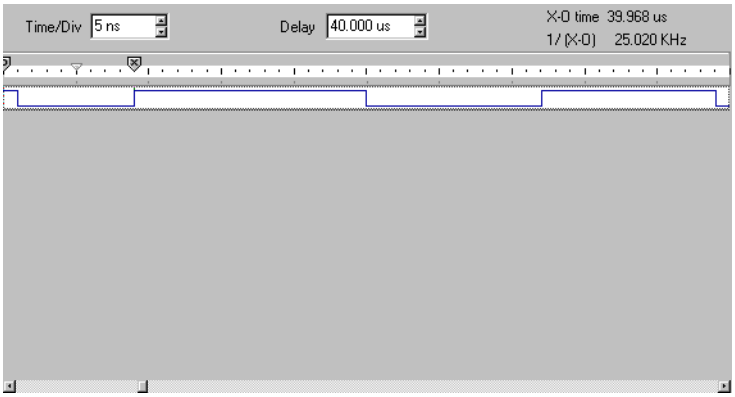
1 Enable the pulse generator channel 2 output (LED off)

2 Acquire and analyze the data.

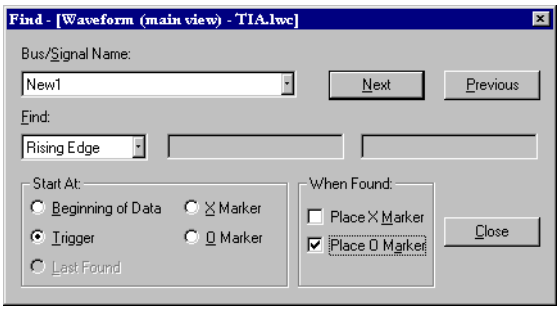
a Set the Time/Div to 5 ns.

b On the PC, push the F5 key to Run.

c Set the Delay to 40.000 us. Drag the x marker to the first rising edge on the left of the display. The marker value pop-up should indicate that the x marker is placed approximately 40.000 us.



d On the PC, select Data, then select Find Data Value. Select Start At: Trigger. Select When Found: Place O Marker. Then select Next.



e Select Close to close the Find Data Value window.

f Read the X-O time. The X-O time should be in the range 39.990 - 40.010 ns. If so, then record a PASS in the “Performance Test Record” on page 64.

Performance Test Record

Agilent Technologies E9340A LogicWave Logic Analyzer	
Serial No._____	Work Order No._____
Recommended Test Interval - 2 Year/4000 hours	Date_____
Recommended next testing_____	Temperature_____

Test	**Settings**	**Results (Pass/Fail)**
Self-Tests	----------	_____
Threshold Accuracy, Pod 1	ECL, ±139 mV	_____
	0 V, ±100 mV	_____
Threshold Accuracy, Pod 2	ECL, ±139 mV	_____
	0 V, ±100 mV	_____
Single-Clock, Single-Edge Acquisition	CLK1 rising	_____
	CLK1 falling	_____
	CLK2 rising	_____
	CLK2 falling	_____
Multiple-Clock, Multiple-Edge Acquisition	CLK1 rising + CLK2 rising	_____
	CLK1 falling + CLK2 falling	_____
Single-Clock, Multiple-Edge Acquisition	CLK1 both edges	_____
	CLK2 both edges	_____
Time Interval Accuracy	----------	_____

4

Troubleshooting

This chapter helps you troubleshoot the logic analyzer.

This chapter consists of troubleshooting hints and procedures. This information is not intended for component-level repair.

The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies sales office for more details.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument.

Troubleshooting Hints

Connecting the logic analyzer to the host PC

- ❏ Use only the HP C2946A parallel cable included with the logic analyzer.
- ❏ Do not use any switchboxes to connect multiple devices, including the logic analyzer, to the host PC.
- ❏ The parallel port on the host PC must not have any other devices connected to it. The parallel port must be free.
- ❏ Ensure the parallel port transfer mode is set to either nibble, byte, or Enhanced Capabilities Port (ECP). Enhanced Parallel Port (EPP) mode is not supported. To verify and change the transfer mode:

  a Reboot the PC and interrupt the boot process using the [F2] key (you must have Administrator privileges on a PC running NT).

  b Scroll down until you see the parallel port configuration.

  Transfer modes reported may not have the names “byte” or “nibble”; however, they may have other names. In this case, consult your PC documentation to resolve the transfer mode name listed with the IBM convention “byte” (that is, Data Out to Data Out, tristated) and “nibble” (that is, Data Out to Status In). However, EPP and ECP modes should be clearly identified.

Starting the application

- ❏ Connect the logic analyzer to the PC and apply power; then, launch the Agilent LogicWave application. The application will search for a parallel port, then it will search for the logic analyzer hardware. If the logic analyzer hardware is not found, you will be prompted to manually search, or to work off-line.

  If you initiate a manual search and the hardware is found, but the user interface is unable to connect to the hardware, it is likely the PC parallel port is in EPP or another unsupported transfer mode. The parallel port transfer mode must be changed using the procedure above.

- ❏ A hardware test is done as part of the Connect process. If the test fails, the logic analyzer module must be replaced. A PASS/FAIL status is reported in

the application startup dialog as the Connect is attempted.

Using LogicWave

- When using the probe tip assembly, ensure there is adequate grounding. At clock speeds close to 100 MHz, the pod ground (5" ground lead) is usually not sufficient. At least 4 channel grounds (2" ground lead), one every four channels, is recommended. More is better.
- Use the test point on the top of the logic analyzer to verify the operation of the individual logic analyzer channels. The LED will blink to indicate if the connected channel is operating properly.
- The online help system requires Microsoft Internet Explorer (MSIE) world-wide web browser version 4.00 or later. If you attempt to access the online help and the browser is not installed, your PC will likely crash. MSIE is included in the installation CD-ROM shipped with the logic analyzer. The browser is also available from Microsoft on the world-wide web at http://www.microsoft.com/windows/Ie/default.htm

Troubleshooting Procedures

To run the self-tests

Self-tests identify the correct operation of major functional areas of the instrument. You can run all self-tests without accessing the interior of the instrument.

1 Start the LogicWave user interface.

The self-tests can run optionally when starting the user interface, after the user interface connects to the logic analyzer.

2 If the self-tests are nor run when starting the user interface, choose the Tools->Self Test... command.

If the self-tests pass, a confirmation dialog appears.

If the self-tests fail, the logic analyzer assembly requires replacement.

To test the auxiliary power

NOTE: The +5V supply is capable of providing only a minimal amount of current.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part Number
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	3478A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.

5

Replaceable Parts

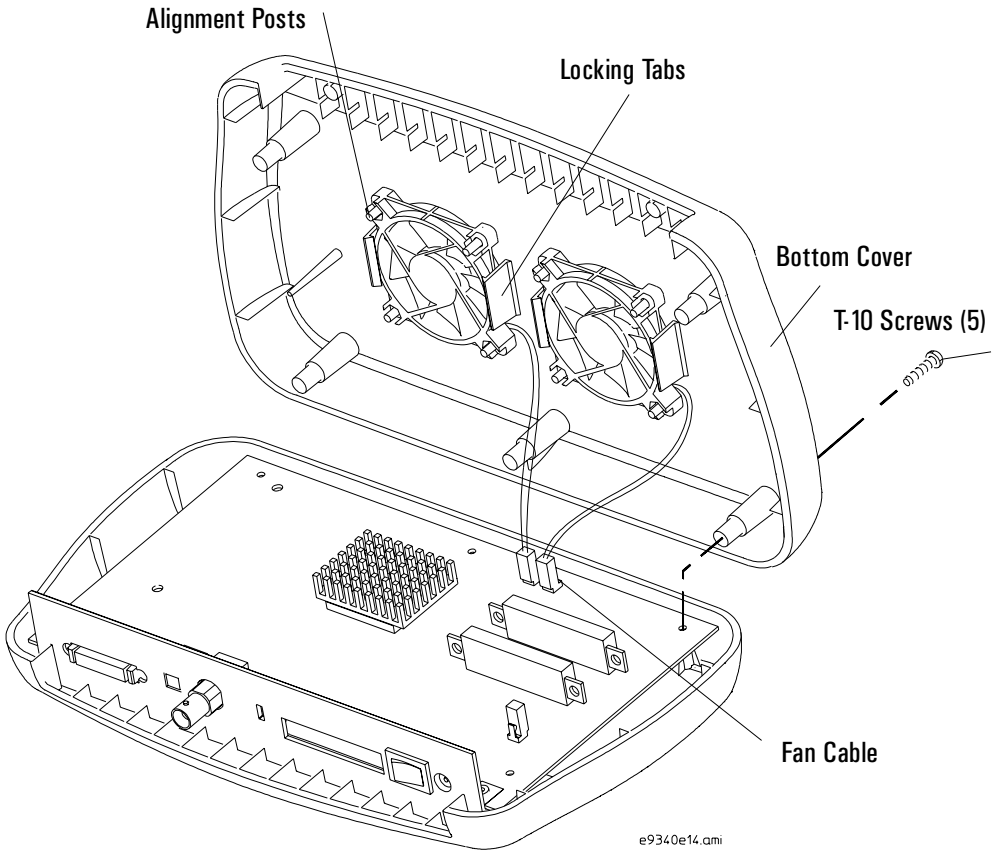
This chapter contains information on replacing assemblies and identifying and ordering replaceable parts for your logic analyzer.

To replace the fan

In case of a hardware failure of the logic analyzer, the entire assembly will be replaced. However, if one or both fans are not operating and the logic analyzer is working, the fans can be replaced.

NOTE: One fan is sufficient to provide adequate cooling for the logic analyzer.

To replace the fan follow this procedure:



1 Disassemble the cover.

a Using a Torx T-10 screwdriver, remove five screws that hold the clamshell cover together.

b Separate the halves of the cover. There are no tabs or anything that hold the cover together in addition to the screws.

2 Remove the fan.

a Unplug the failed fan from the logic analyzer circuit board.

CAUTION: There are two locking tabs, one on either side of the fan, that hold the fan onto the bottom clamshell cover. When removing the failed fan, be careful not to break these tabs.

b Using your thumb, gently push back one tab while gently attempting to lift the fan away from the bottom cover. After the side of the fan is raised approximately 2-3 mm, gently push back the second tab with your thumb while lifting the other side of the fan.

c Keep repeating step b until the fan has cleared the tabs and can be lifted out of the bottom cover.

3 Install the replacement fan.

The fan is installed so that air flows out of the cabinet.

a Orient the fan into the bottom cover as shown in the picture.

b Align the mounting holes in the corners of the fan frame with the alignment posts in the bottom cover.

c Gently apply force straight down on the fan until the locking tabs spread, the fan slides down the alignment posts, and the fan locks in place in the bottom cover.

d Plug the fan cable into the logic analyzer circuit board.

4 Reassemble the cover.

a Lay the bottom clamshell cover upright on the workbench.

b Position the top cover over the bottom cover, then lower the top cover onto the bottom cover. There are no tabs that hold the covers together, so they should assembly easily.

c While holding the two covers together, turn the assembly over.

d Install five screws that secure the two covers together.

To return assemblies

Before shipping the logic analyzer or assemblies to Agilent, contact your nearest Agilent Technologies sales office for additional details.

1. Write the following information on a tag and attach it to the part to be returned.
   - Name and address of owner
   - Model number
   - Serial number
   - Description of service required or failure indications
2. Remove accessories from the logic analyzer.

   Only return accessories to Agilent if they are associated with the failure symptoms.
3. Package the logic analyzer.

   You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION: For protection against electrostatic discharge, package the logic analyzer in electrostatic material.

4. Seal the shipping container securely, and mark it FRAGILE.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies sales office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies sales office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies sales office.

Within the USA, Agilent can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies sales office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Agilent to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies sales office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

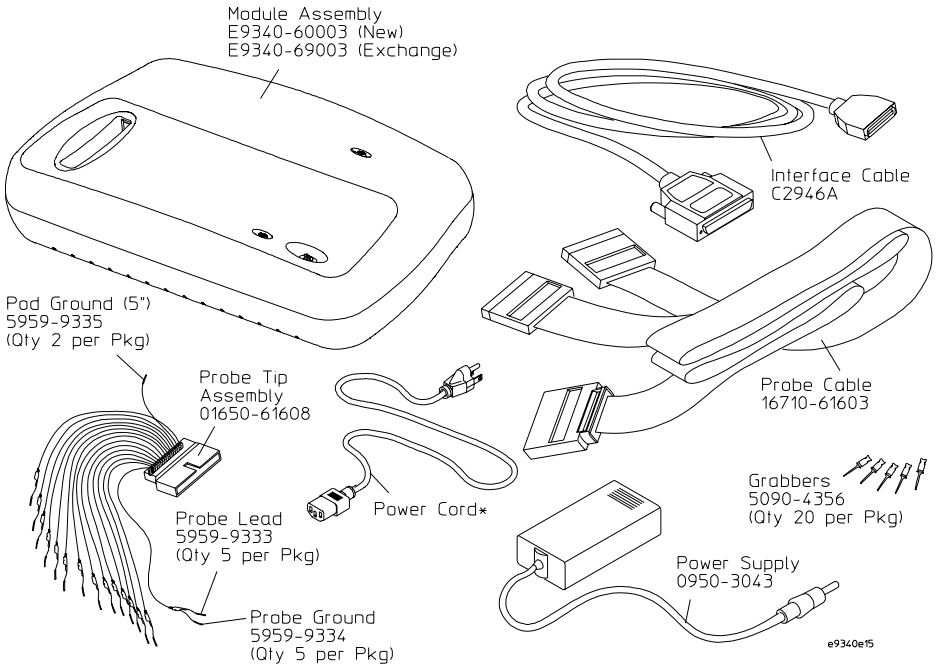
Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent.

After you receive the exchange assembly, return the defective assembly to Agilent. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies sales office for information.

Exploded View

Exploded view of the LogicWave logic analyzer.



Power Cord Part Number	Description
8120-1521	Power Cord-United States (7.5 ft)
8120-1703	Power Cord (Option #900-UK)
8120-0696	Power Cord (Option #901-Austl)
8120-1692	Power Cord (Option #902-Europe)
8120-2296	Power Cord (Option #906-Swit)
8120-2957	Power Cord (Option #912-Den)
8120-4600	Power Cord (Option #917-Africa)
8120-4754	Power Cord (Option #918-Japan)
8120-6799	Power Cord (Option #919-Israel)
8120-6871	Power Cord (Option #920-Argentina)
8120-6979	Power Cord (Option #921-Chile)
8120-8377	Power Cord (Option #922-China)

Index

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	Agilent Technologies
Manufacturer's Address:	Digital Design Product Generation Unit 1900 Garden of the Gods Road Colorado Springs, CO 80907 USA

declares, that the product

Product Name:	Logic Analyzer
Model Number(s):	E9340A
Product Option(s):	All

conforms to the following Product Specifications:

Safety:	IEC 1010-1:1990+A1+A2:1995 / EN 61010-1:1993	
	UL3111	
	CSA-C22.2 No. 1010.1:1993	
EMC:	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 555-2:1982 + A1:1985 / EN 60555-2:1987	
	IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991	
	IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
	IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
	IEC 801-4:1998 / EN 50082-1:1992	0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE marking accordingly.

This product was tested in a typical configuration with Agilent Technologies test systems.

Colorado Springs, 9/10/99

Ken Wyatt

Ken Wyatt, Product Regulations Manager

European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

Product Regulations

Safety

IEC 1010-1:1990+A1 / EN 61010-1:1993
UL3111
CSA-C22.2 No. 1010.1:1993

EMC

This Product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.

CE
ISM 1-A

Emissions

EN55011/CISPR 11 (ISM, Group 1, Class A equipment),
IEC 555-2 and IEC 555-3

Immunity

EN50082-1	Code[1]
IEC 801-2 (ESD) 8kV AD	3
IEC 801-3 (Rad.) 3 V/m	1
IEC 801-4 (EFT) 1kV	1

[1]Performance Codes:
1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

Restricted Rights Legend

Use, duplication, or disclosure by the U.S. Government is subject to restrictions set forth in subparagraph (C) (1) (ii) of the Rights in Technical Data and Computer Software Clause in DFARS 252.227-7013. Agilent Technologies, 3000 Hanover Street, Palo Alto, CA 94304 U.S.A. Rights for non-DOD U.S. Government Departments and Agencies are set forth in FAR 52.227-19 (c) (1,2).

Document Warranty

The information contained in this document is subject to change without notice.

Agilent Technologies makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability or fitness for a particular purpose.

Agilent Technologies shall not be liable for errors contained herein or for damages in connection with the furnishing, performance, or use of this material.

Safety

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warning

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

Agilent Technologies
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901-2197, U.S.A.

Product Warranty

This Agilent Technologies product has a warranty against defects in material and workmanship for a period of three years from date of shipment. During the warranty period, Agilent Technologies will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies.

For products returned to Agilent Technologies for warranty service, the Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instructions when properly installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer- supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. Agilent Texhnologies specifically disclaims the implied warranties of merchantability or fitness for a particular purpose.

Exclusive Remedies

The remedies provided herein are the buyer's sole and exclusive remedies. Agilent Technologies shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Agilent Technologies products. For any assistance, contact your nearest Agilent Technologies Sales Office.

Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory. Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

About this edition

This is the *Agilent Technologies LogicWave (E9340A) Service Guide*.

Publication number
E9340-97001, December 1999
Printed in USA.

Print history is as follows:
First edition, December 1999

New editions are complete revisions of the manual. Many product updates do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.